REMARKS

None of the claims have been amended or cancelled herein. Claims 13 and 14 have been added. Claims 1, 7, 13 and 14 are the independent claims. In view of the above, it is respectfully submitted that claims 1-14 are pending. No new matter is presented and entry and reconsideration are respectfully requested.

Regarding newly added claim 13, it is noted that claim 13 is drawn to a thin film transistor (TFT) comprising a lightly doped drain (LDD) region or offset region, wherein the thin film transistor is formed so that primary crystal grain boundaries of a polysilicon substrate are positioned in channel, source and drain regions but not positioned in the LDD or offset region. None of the references cited in the Office Action teach or suggest such novel features and therefore, Applicants respectfully assert that claim 13 is allowable.

Regarding newly added claim 14, it is noted that claim 14 is drawn to a flat panel display device comprising: a thin film transistor including an LDD region or offset region, wherein the thin film transistor is formed so that primary crystal grain boundaries of a polysilicon substrate are positioned in a channel, source and drain regions but not positioned in the LDD or offset region. None of the references cited in the Office Action teach or suggest such novel features and therefore, Applicants respectfully assert that claim 14 is allowable.

DRAWINGS:

In the Office Action at page 2, the Examiner objected to the drawings under 37 CFR 1.83(a). In order to overcome these objections, a replacement figure is submitted herewith. Furthermore, although the Office Action indicates that the drawings fail to show every feature of the invention specified in the claims, Applicants note that all such features are illustrated in the drawings. In particular, the primary crystal grain boundaries are shown inclined to a current direction between active channel regions of the thin film transistor at an angle of $-45° \leq \Theta \leq 45°$, as illustrated in FIGS. 2A and 2B.

Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

REJECTIONS UNDER 35 U.S.C. 102:

Claims 1, 2, 4, 7, 8, and 10 are rejected under 35 U.S.C. §102(e) as being anticipated by Isobe et al. (U.S. Patent No. 6,890,840).

Regarding the rejection claim 1, it is noted that claim 1 recites a thin film transistor (TFT) comprising a lightly doped drain (LDD) region or offset region, wherein the thin film transistor is formed so that primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD or offset region. Applicants respectfully assert that Isobe fails to teach or suggest each of these features. For support, Applicants note that Isobe does not, in fact, disclose this subject matter, notwithstanding the statements of the Examiner to the contrary.

In detail the Office Action states that Isobe discloses that the crystal aggregate boundaries are located outside of the TFT formation region and that the aggregate boundaries are the primary grain boundaries. However, a review of Isobe shows the formation of a channel formation region, or a TFT formation region, using one crystal aggregate (domain) by controlling crystal location and size, thus suppressing TFT variations. Each TFT formation region is isolated, a metallic element for promoting crystallization (typically Ni) is added, and heat treatment is performed, thus making it possible to arbitrarily determine the locations of crystal aggregates (domains) (abstract). In other words, Isobe discloses a method for forming a channel formation region using a metal induced lateral crystallization (MILC) method.

As noted in the previous response dated October 13, 2005, an MILC method cannot form primary crystal grain boundaries and therefore since Isobe discloses using an MILC method, Isobe fails to teach or suggest primary crystal grain boundaries as well as the other features recited in independent claim 1. Support for such statement can be found in U.S. Patent No. 6,274,888 to Suzuki which describes a method of growing crystals using an MILC method (see FIGS. 4A-4D, 7A-7D, 8A-8F and 9A-9F and column 8, lines 26-50). The MILC method disclosed by Suzuki includes forming a first a-Si thin film 11 on a substrate 3, depositing a metal film 14 on the first a -Si thin film and forming an opening 15 in the metal film 14. After several processes, the a-Si film 11 under the metal film 14 is transformed into the p-Si film 16, and then the lateral growth of the crystalline grains occurs. In other words, the metal film 14 is absorbed completely by the a-Si film. To continue crystal growth, a second a-Si film is deposited over the entire area and irradiation

of excimer laser onto the a-Si film 18 crystallizes the a-Si film 18 and so forth (column 9, lines 18-65). Accordingly, in the MILC method, the continuous application and treatment of films over the crystal, prevents formation of primary crystal grain boundaries. As noted above, Isobe discloses such an MILC method and thus cannot form primary crystal grain boundaries as recited in independent claim 1.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 102(e) should be withdrawn because Isobe fails to teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 2 and 4 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2 and 4 also distinguish over the prior art.

Regarding the rejection of claim 7, it is noted that claim 7 recites a flat panel display device comprising, a thin film transistor comprising an LDD region or offset region, wherein the thin film transistor is formed so that primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD or offset region. Applicants respectfully assert that Isobe fails to teach or suggest each of these features.

As noted above, Isobe discloses a method of forming a channel formation region, or a TFT formation region, using one crystal aggregate (domain) by controlling crystal location and size, thus suppressing TFT variations, using an MILC method. As also noted above, in an MILC method primary crystal grain boundaries cannot be formed and therefore Isobe fails to teach or suggest primary crystal grain boundaries.

Accordingly, Applicants respectfully assert that the rejection of claim 7 under 35 U.S.C. § 102(e) should be withdrawn because Isobe fails to teach or suggest each feature of independent claim 7.

Furthermore, Applicants respectfully assert that dependent claims 8 and 10 are allowable at least because of their dependence from claim 7, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 8 and 10 also distinguish over the prior art.

REJECTIONS UNDER 35 U.S.C. §103:

Claims 1-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Zhang et al. (U.S. Patent 5,563,426) in view of Suzuki et al. (U.S. Patent 6,274,888).

Regarding the rejection of claim 1, it is noted that claim 1 recites a thin film transistor (TFT) comprising a lightly doped drain (LDD) region or offset region, wherein the thin film transistor is formed so that **primary crystal grain boundaries** of a polysilicon substrate are not positioned in the LDD or offset region.

The Office Action states that Zhang discloses a TFT formed so that primary crystal grain boundaries 4 of a polysilicon substrate are formed outside the TFT formation regions (FIGS. 1B, 1C and 4C). The Office Action recognizes that Zhang fails to teach an LDD region and relies on Suzuki for such teaching. Applicants respectfully assert that the combination of Zhang and Suzuki fails to disclose each of these features and furthermore there is no teaching or suggestion to combine these references to teach the feature of independent claim 1.

Zhang discloses a method of manufacturing a TFT using a crystal silicon film obtained by crystallizing an amorphous silicon film using a plurality of island nickel films (column 11, lines 21-22). The TFT includes island nickel regions 2, portions 3, inter-crystalline boundaries 4, an intermediate region 5, a semiconductor region 6 and a gate wire 7 (column 12, lines 25-55; FIGS. 1A-1C). In other words, Zhang discloses a method of manufacturing a TFT using metal induce lateral crystallization (MILC). As noted above, in an MILC method primary crystal grain boundaries cannot be created and therefore, although Zhang discloses inter-crystalline boundaries 4, these boundaries are not primary crystal grain boundaries and they are not positioned in the LDD region, as recited in independent claim 1.

As noted above, Suzuki also discloses a TFT manufactured using an MILC method, and thus Suzuki also fails to teach or suggest thin film transistor formed so that **primary crystal grain boundaries** of a polysilicon substrate are not positioned in the LDD or offset region, as recited in independent claim 1.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 103(a) should be withdrawn because neither Zhang nor Suzuki, whether taken singly or combined, teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 2-6 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2-6 also distinguish over the prior art.

Regarding the rejection of independent claim 7, it is noted that claim 7 recites a flat panel display device comprising, a thin film transistor comprising an LDD region or offset region, wherein the thin film transistor is formed so that primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD or offset region. Applicants respectfully assert that the combination of Zhang and Suzuki fails to disclose each of these features and furthermore there is no teaching or suggestion to combine these references to teach the feature of independent claim 7.

As noted above, although Zhang discloses inter-crystalline boundaries 4, these boundaries are not primary crystal grain boundaries and they are not positioned in the LDD region, as recited in independent claim 7.

As also noted above, Suzuki fails to cure the deficiencies of Zhang since Suzuki describes a method of growing crystals using an MILC method, which is a method known for not creating primary crystal boundaries.

Accordingly, Applicants respectfully assert that the rejection of claim 7 under 35 U.S.C. § 102(e) should be withdrawn because neither Zhang nor Suzuki, whether taken singly or combined teach or suggest each feature of independent claim 7.

Furthermore, Applicants respectfully assert that dependent claims 9-12 are allowable at least because of their dependence from claim 7, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 9-12 also distinguish over the prior art.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding rejections have been overcome and/or rendered moot. And further, that all pending claims patentably distinguish over the prior art. There being no further outstanding rejections, the application is submitted as being in condition for allowance which action is earnestly solicited.

If there are any additional fees associated with filing of this Preliminary Amendment, please charge the same to our Deposit Account No. 50-3333.

Respectfully submitted,

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